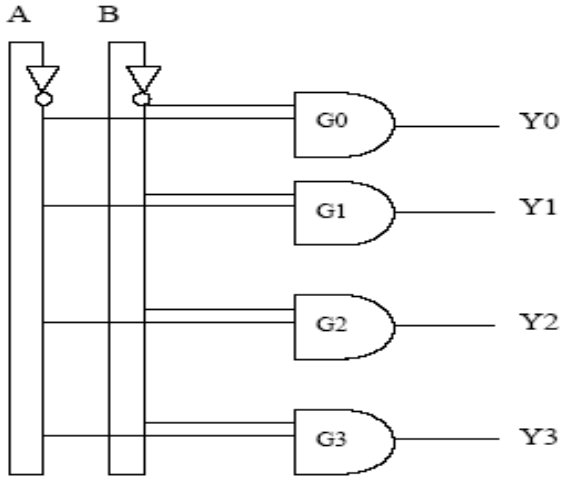
UNIT IV

4.1 DIGITAL COMPONENTS: INTEGRATED CIRCUITS

- Integrated circuit(IC) is a small silicon semiconductor crystal is called a chip
- The various gates are interconnected inside the chip to form the required circuit.
- Each IC has a numeric designation printed on the surface of the package for identification.
- Small Scale Integration (SSI) devices contain several independent gates in a single package.
- The inputs and outputs of the gates are connected directly to the pins in the package.
- Medium Scale Integration (MSI) devices have a complexity of approximately 10 to 200 gates in a single package.
- Large Scale Integration (LSI) devices contain between 200 and few thousand gate in a single package
- Very Large Scale Integration (VLSI) devices contain thousands of gate in a single package

4.1.1 DECODERS

- A *decoder* is a combinational circuit that converts binary information from '*n*' input lines to a maximum of 2^n unique output lines.
- It is used to decode the binary information to some other number system (decimal or hexadecimal).



A 2 to 4 line Decoder

Inputs			Outputs							
A	B	C	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

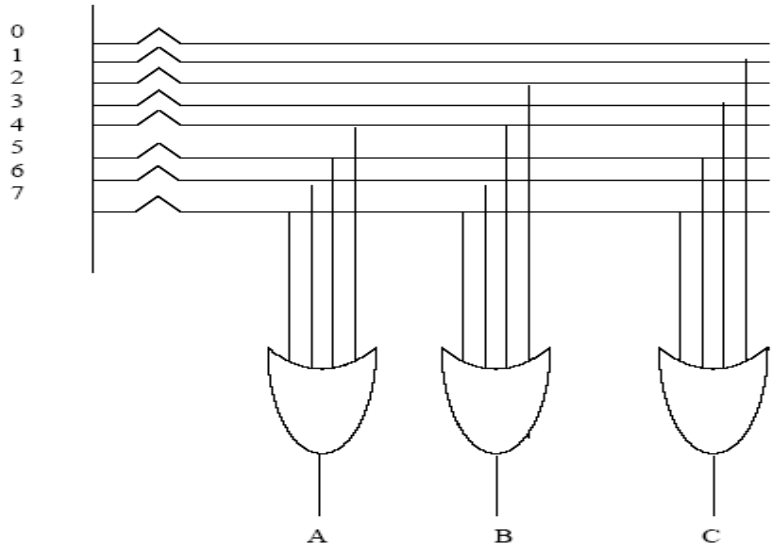
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	1	0	0	0
1	0	0	0	0	0	1	0	0	0	0
1	0	1	0	0	1	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0

Truth Table for 3 to 8 line decoder

- Here, a 3 bit binary information is decoded into eight outputs.
- The three NOT gates or invertors on the input side give the complement of the inputs.
- The eight AND gates are used to active the outputs ‘High’.
- It is also called as binary to octal decoder.
- The applications of decoder is binary to octal conversion.
- It is also used to display the letters of the alphabet.
- Light Emitting Diodes (LEDs) are used as light source for the read-out display.

4.1.2 ENCODERS

- It is just reverse process of decoding.
- This changes decimal signals into equivalent binary signals.
- It is also called as coder.
- It has 2^n or less input lines and n output lines.
- The octal to binary encoder has 8 inputs and three outputs.
- It is constructed using three OR gates.

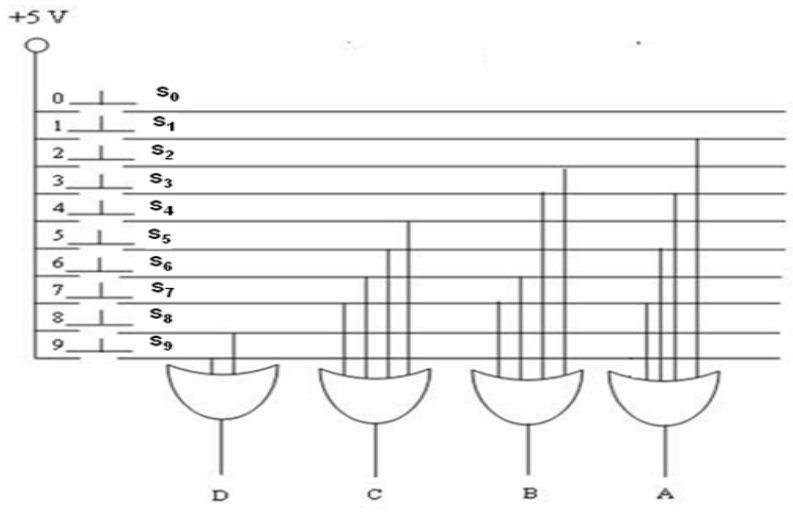


Octal to binary encoder

Inputs								Outputs		
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	A	B	C
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

Truth Table for Octal to binary encoder

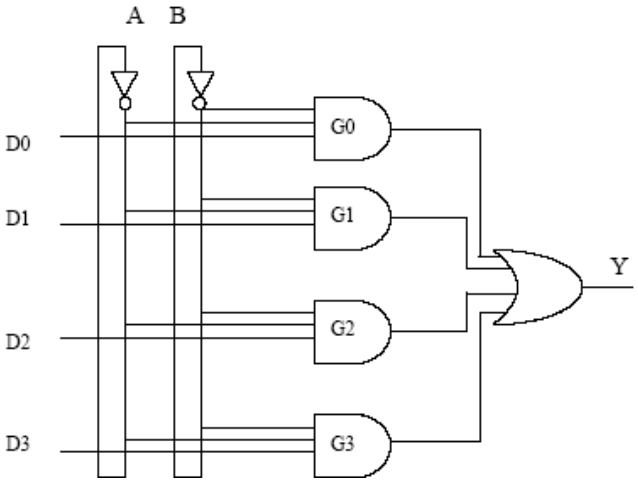
- Decimal to BCD encoder can be constructed using four OR gates.
- This encoder has 10 input lines and four output lines.
- The switches S_0 to S_9 are push buttons.
- When push-button S_2 corresponding to decimal number 2 is pressed, the OR gate for output B has a high input, therefore the output BCD word is given by
    - D C B A = 0 0 1 0.



Decimal to BCD encoder

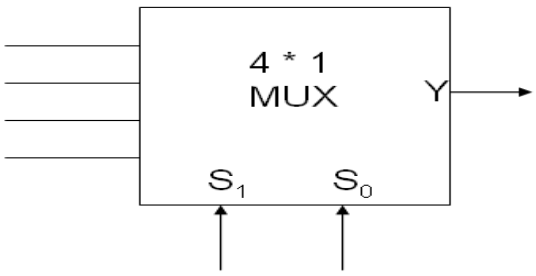
4.1.3 MULTIPLEXERS

- It is also known as data selector and abbreviated as MUX.



- It is a combinational logic circuit.
- It accepts several data inputs and selects only one at a time and directs it to a single output line.

4-to-1 line Multiplexer



Block Diagram of MUX

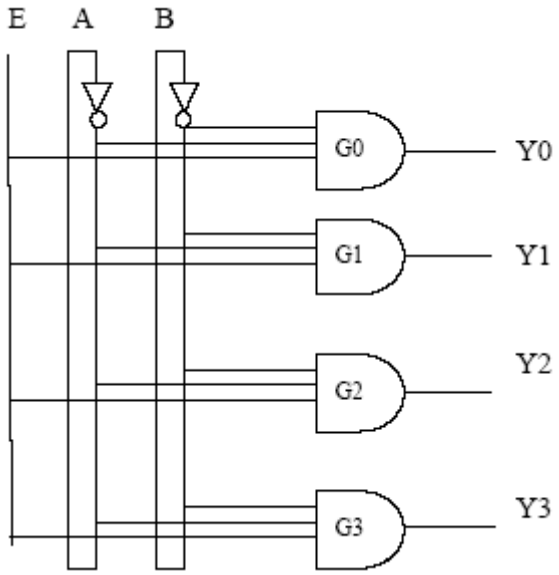
Select		Output
S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

Function Table

- In 4 –to-1 line multiplexer, there are four inputs I_0, I_1 , I_2 and I_3 which is applied to one input of an AND gate.
- The two select inputs S_1 and S_2 are decoded to select a particular AND gate.
- The outputs of the AND gates are applied to the single OR gate to provide the single output.
- When S_1 S_0 = 11, the AND gate associated with I_3 has two of its input equal to 1. The third input is connected to I_3 . The other three AND gates have atleast one input equal to zero. So the OR gate output is now equal to the value of I_3, thus providing a path from select input to output.
- The size of the multiplexer is given by 2^n to 1 line, where 2^n stands for the number of the input lines and n stands for the number of select inputs.

4.1.4 DEMULTIPLEXERS

- It is also known as data distributor and abbreviated as DEMUX.
- It does the reverse process of the multiplexer.
- It takes in single input and distributes several outputs.
- It receives single line information and transmits it to one of 2^n possible output lines.
- The select input will determine or decide to which output the data input will be transmitted.



DEMULTIPLEXERS

- There is a single input line I which is connected to all the AND gates.
- Three select inputs are used , so n=3.
- There must be 2^n output lines (2^3=8).
- The select inputs enable one of the eight AND gates.
- Demultiplexers are useful when information from one source is to be fed to several places.

Inputs				**Outputs**							
Data Input	Select			Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
	S_2	S_1	S_0								
I	0	0	0	0	0	0	0	0	0	0	I
I	0	0	1	0	0	0	0	0	0	I	0
I	0	1	0	0	0	0	0	0	I	0	0
I	0	1	1	0	0	0	0	I	0	0	0
I	1	0	0	0	0	0	I	0	0	0	0
I	1	0	1	0	0	I	0	0	0	0	0

I	1	1	0	0	I	0	0	0	0	0	0
I	1	1	1	I	0	0	0	0	0	0	0

Truth Table for 1 to 8 line Demultiplexer

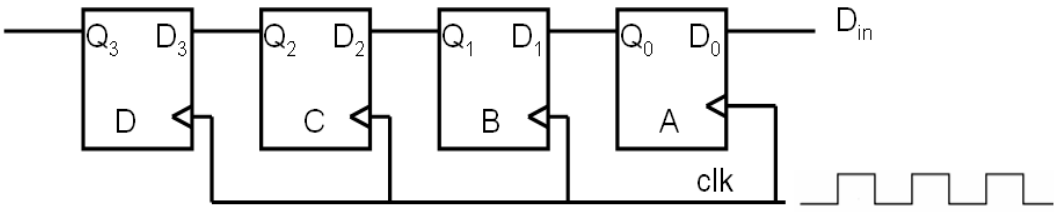
4.2 REGISTERS

- Register is a group of cascaded flip-flops for storing binary information momentarily.
- They are used in microprocessors and digital computers.
- They are used for transfer of binary information and for storage of binary data which is being decoded in digital systems.

4.2.1 SHIFT REGISTERS

- Shift register is a register, which is used to assemble and store the information arriving from a serial source.
- A shift register can shift binary word either to the left or to the right.
- It consists of cascaded flip-flops, with the output of each flip-flop connected to the input of the next flip-flop.
- A common clock pulse is applied to all the flip-flops, clocking them synchronously and causing the shift from one stage to the next stage.
- The shift register is a synchronous sequential circuit.
- When a shift register is used to move the stored bits to the left, it is called shift-left register.
- When a shift register is used to move the stored bits to the right, it is called shift-right register.

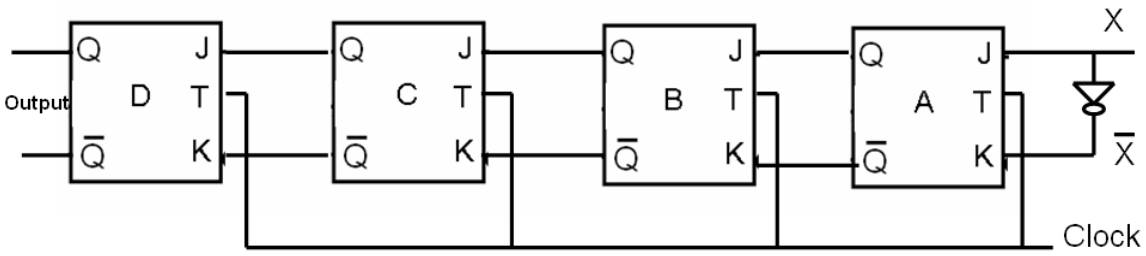
SHIFT-LEFT REGISTER



Shift-left register using D flip-flop

- In shift-left register,the data input D_{in} is applied to flip flop A.
- A common edge triggered clock pulse is applied to all the four flip flops.
- The data input D_{in} sets up the first flip-flop A, whose output Q_0 sets the second flip-flop, whose output Q_1 sets the third flip-flop C and so on.

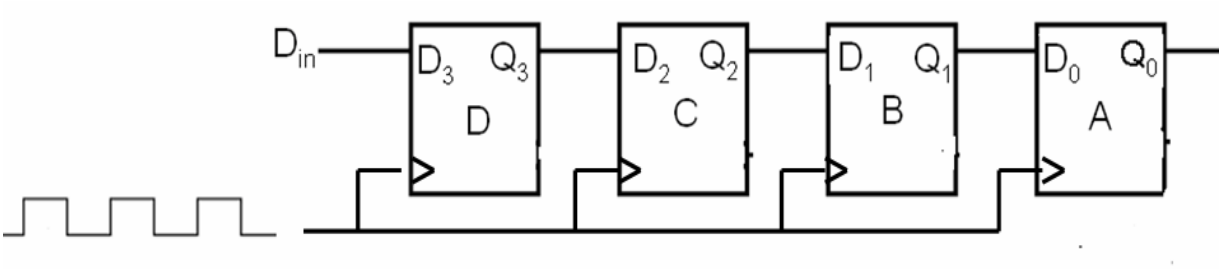
- On arrival of the next positive clock edge, the stored bits move one position to the left.
- Initially Q = D C B A = 0 0 0 0 and D_{in} = 1
- The first rising clock edge will set the right flip-flop A and stored word becomes Q = D C B A = 0 0 0 1
- Now the input to the D_1 to the flip-flop B is equal to '1'. On arrival of the next positive clock edge, flip-flop B sets and the contents of the register becomes Q = D C B A = 0 0 1 1
- The third positive clock edge gives the output Q = D C B A = 0 1 1 1



Shift-left register using JK flip-flop

- The data input X is connected to J input and $\overline{X}$ obtained after inversion is connected to K input.
- The clock pulse is applied at the T inputs of all the flip-flops simultaneously.
- When the first clock pulse arrives, the data inputs X and $\overline{X}$ are shifted to the output of the flip-flop A.
- Thus on arrivals of each clock pulse, the data are shifted to the output of the next flip-flop.

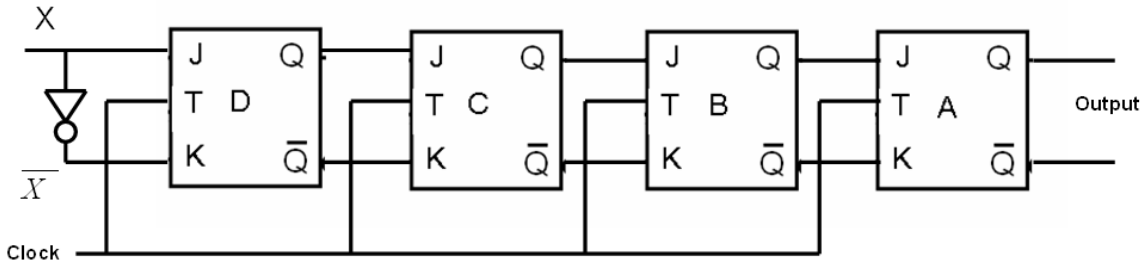
SHIFT-RIGHT REGISTER



Shift-right register using D flip-flop

- The connection is similar to shift-left register with only difference that the data input is connected to D flip-flop and output is taken from A flip-flop.
- A common edge triggered clock pulse is applied to all the four flip flops.
- The output Q_3 of flip-flop D, sets the input for the prededing flip-flop C.
- When the positive clock edge arrives, the stored bit move one position to the right.
- Initially Q = D C B A = 0 0 0 0 and D_{in} = 1

- The first rising clock edge will set the left flip-flop D and stored word becomes Q = D C B A = 1 0 0 0.
- The second positive clock edge gives the output Q = D C B A = 1 1 0 0
- The third positive clock edge gives the output Q = D C B A = 1 1 1 0
- The fourth positive clock edge gives the output Q = D C B A = 1 1 1 1
- The word is stored and remains unchanged till D_{in} = '1'.



Shift-right register using JK flip-flop

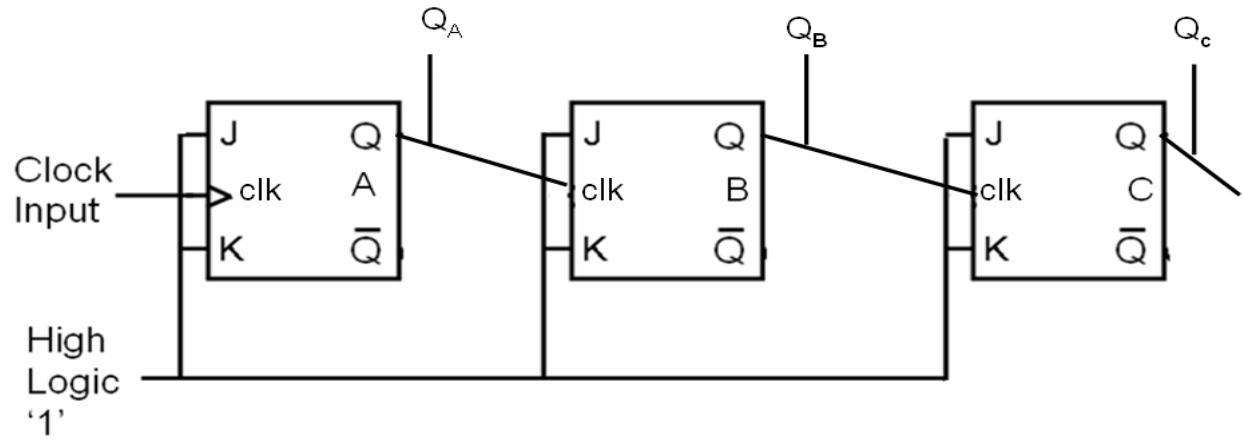
- The data input X is connected to J input and $\overline{X}$ obtained after inversion is connected to K input.
- The clock pulse is applied at the T inputs of all the flip-flops simultaneously.
- When the first clock pulse arrives, the data inputs X and $\overline{X}$ are shifted to the output of the flip-flop D.
- Thus on arrival of each clock pulse, the data are shifted to the output of the next flip-flop.
- Four types of shift registers are
    1. Serial in serial out shift registers
    2. Parallel in serial out shift registers
    3. Serial in parallel out shift registers
    4. Parallel in parallel out shift registers
    5. Parallel in parallel out bi-directional shift registers

4.3 COUNTERS

- The counter has the ability to count.
- It is an important and useful subsystem of a digital system.
- A counter is a group of cascaded flip-flops to store more binary information.
- A counter is a register, which is capable of counting the number of clock pulses, which has arrived at its clock input.
- It is used in control systems, computers, electronic and scientific instruments.
- The application of counters includes counting the occurrence of events, frequency division, time sequence of operation of equipments and digital systems.
- Two types of counters are
    i) asynchronous or ripple counter
    ii) synchronous counter.

ASYNCHRONOUS COUNTER

- It is an asynchronous sequential circuit.
- All the flip-flops in an asynchronous counter are not under the control of same clock pulse.
- An n-bit binary ripple counter can count upto a maximum of 2^n states.
- A ripple counter is a basic and simple counter.
- It has limitation on speed of operation.



3 bit binary ripple counter

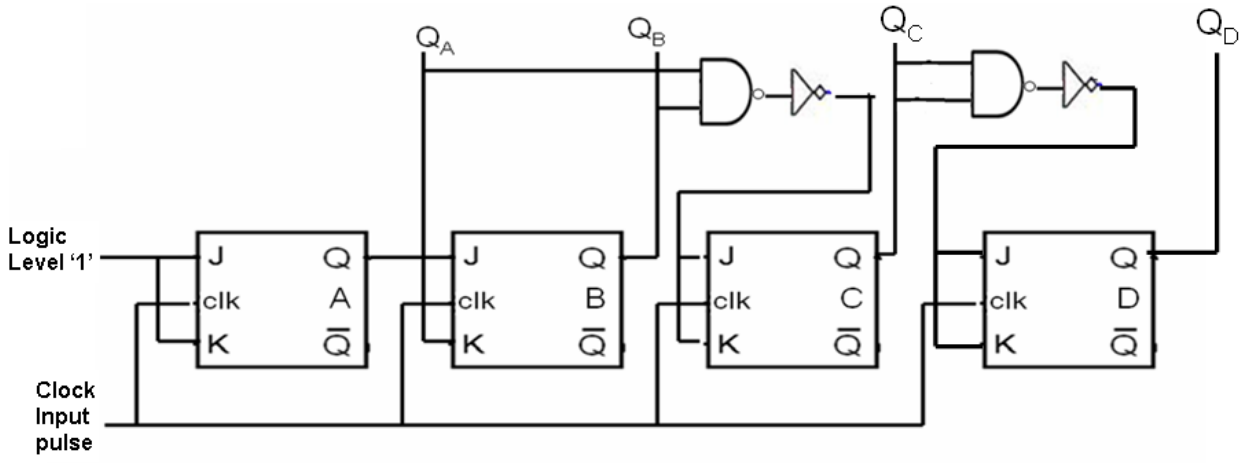
- In 3 bit binary ripple counter, three JK flip-flops are connected in cascade.
- It can count upto 2^3 states i.e 8 states.
- Initially all the four flip-flops A,B and C are in logic '0' state.
- A clock pulse is applied to flip-flop A only, which makes Q_A to change from logic 0 to logic 1 state. Other flip-flops B and C do not change their state. After the application of the clock pulse to the clock input, the counter reads.
    - $Q = Q_C\ Q_B\ Q_A = 0\ 0\ 1$
- When second clock pulse is applied to flip-flop A, output Q_A changes state from logic 1 to logic 0. Due to this state change, a negative going pulse created at Q_A , which is connected to clock input of the flip-flop B. This pulse triggers the flip-flop B and changes the state of Q_B from 0 to 1. Flip flop C do not change its state. Now the counter reads
  $Q = Q_C\ Q_B\ Q_A = 0\ 1\ 0$
- The counter will continue to count the input clock pulses in the binary form upto the state till Q_C , Q_B and Q_A all become high. That is the counter reads $Q = Q_C\ Q_B\ Q_A = 1\ 1\ 1$, which in decimal means that it will count upto 7 clock pulses.
- On the arrival of the 8^{th} clock pulse, all the three flip-flops will go to '0' and the counter will once again repeat its counting from 000 to 111 (from 0 to 7).

SYNCHRONOUS COUNTER

- It is an synchronous sequential circuit.
- All the flip-flops in an asynchronous counter are under the control of same clock pulse.
- It is used to eliminate the cumulative flip-flop delays.
- Two methods are used to control the flip-flop in synchronous counter.

- one with ripple carry
- one with parallel carry
- All the flip-flops in synchronous counter change their state simultaneously and thus They are capable of operating at higher frequencies and speed.
- They are more complicated and require more components.

(i) Four-bit synchronous counter with serial or ripple carry



- Four-bit synchronous counter used positive edge triggered JK flip-flop with serial or ripple carry.
- It requires two input logic gates.
- On the arrival of clock pulse, all the flip-flops changes their state simultaneously.
- Inputs of flip-flops are

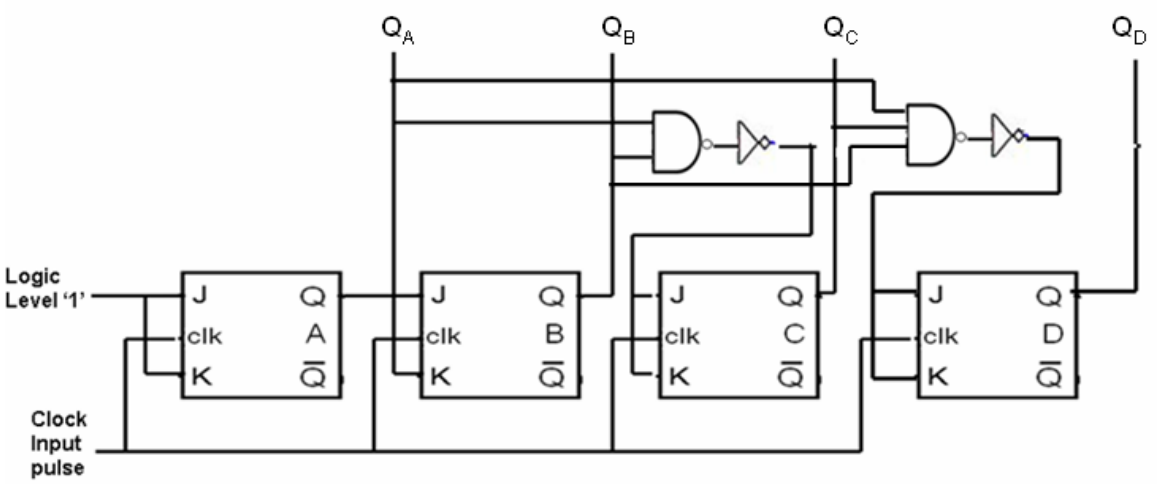
  $J_A = K_A = 1$

  $J_B = K_B = Q_A$

  $J_C = K_C = Q_A * Q_B$

  $J_D = K_D = Q_B * Q_C$

(ii) Four-bit synchronous counters with parallel carry or look-ahead carry



- Here, the state of the flip-flop is fed parallel to all succeeding flip-flops.
- The input clock pulse drive all the flip-flops in parallel.
- The flip-flop A has its J-K inputs to a high voltage level '1' and it responds to each positive clock pulse.
- The remaining flip-flops respond to the next positive clock edge only if all the lower bits are '1's.
- Inputs of flip-flops are

  $J_A = K_A = 1$

  $J_B = K_B = Q_A$

  $J_C = K_C = Q_A * Q_B$

  $J_D = K_D = Q_A * Q_B * Q_C$

4.4 MEMORY UNIT

- Memory stores such binary information as instructions and data, and provides that information to the microprocessor whenever necessary.
- To execute programs the microprocessor reads instructions and data from memory and
- performs the computing operations in its ALU section.
- Results are either transferred to the output section for displayer stored in memory for later use. The memory block has two sections
- Read only memory (ROM)
- Read/Write memory (R/WM), popularly known as Random-Access memory (RAM).
- The ROM is used to store programs that do not need alterations. The monitor program of a single board microcomputer is generally stored in the ROM.
- This program interprets the information entered through a keyboard and provides equivalent binary digits of the microprocessor.

MAIN MEMORY

- The main memory is the central storage unit in a computer system.
- t is a relatively large
  and fast memory used to store programs and data during the computer operation.
- The principal
  technology used for the main memory is based on semiconductor integrated circuits.
- Integrated
  circuit RAM chips are available in two possible operating modes, static and dynamic.
- The static RAM consists essentially of internal flip-flops that store the binary information.
- The stored information remains valid as long as power is applied to the unit.
- The dynamic RAM stores the
  binary information in the form of electric charges that are applied to capacitors.
- he capacitors are provided inside the chip by MOS transistors.
- The stored charges on the capacitors tend todischarge with time and the capacitors
- must be periodically recharged by refreshing the dynamic memory.
- Refreshing is done by cycling through the words every few milliseconds to restore the decaying charge.
- The dynamic RAM offers reduced power consumption and larger storage capacity in a single memory chip.
  it is necessary to combine a number of chips to form the required memory size.
- To demonstrate the chip interconnection, we will show an example of a 1024 * 8 memory constructed with 128 * 8 RAM chips and 512 * 8 ROM chips.